Operation Guide

Brief Guide of PPAP-1610

PPAP-1610 is a Communication Appliance computing board based on VIA VT82C686B chipset technology. PPAP-1610 has three on-board LAN ports to serve communication appliances, such as Firewall, which needs three Ethernet ports to connect external network (internet), demilitarized zone and internal network. Different I/O management policies can be applied respectively to individual network to achieve the highest security level. The target market segment is communication appliance including Virtual Private Network, Load Balancing, Quality of Service, Intrusion Detection, Virus Detection, Firewall and Voice Over IP.

This PPAP-1610 system board is eligible with VIA C3 processor EBGA package (Eden Esp5000) and 144-pin SODIMM up to 512MB DRAM. The enhanced on-board PCI IDE interface supports 2 drives up to PIO mode 4 timing and Ultra DMA/100 synchronous mode feature. The on-board super I/O chipset integrates two serial ports driven by two high performance 16550C-compatible UARTs to provide 16-byte send/receive FIFOs. Besides, the two Universal Serial Bus ports provide high-speed data communication between peripherals and PC.

The on-board flash ROM is used to make the BIOS update easier. The high precision Real Time Clock/Calendar is built to support Y2K for accurate scheduling and storing configuration information. All of these features make PPAP-1610 excellent in stand-alone applications.

If any of these items is damaged or missing, please contact your vendor and save all packing materials for future replacement and maintenance.



Figure 1 PPAP-1610 Board

System Architecture

The following illustration of block diagram will show you how PPAP-1610 gives you a highly integrated system solution. The most up-to-date system architecture of PPAP-1610 includes two main VLSI chips. It contains VIA 8601 and VIA VT82C686B to support VIA C3 processor, SODIMM, USB port, SMBus communication and Ultra DMA/100 IDE Master. The on-board super VIA VT82C686B supports two UARTs and hardware monitoring.

PPAP-1610 has built-in onboard VIA C3 processor EBGA package (Eden Esp5000) 100 or 133MHz system bus) for cost-effective and high performance application.

The VIA 8601 provides a completely integrated solution for the system controller and data path components in a VIA C3 processor system. It provides optimized 64-bit DRAM interface with one 144-pin 3.3V DIMM.

The VIA VT82C686B provides a highly integrated multifunction for the best industry applications. It supports 2-channel dedicated Ultra ATA/33/66/100 IDE master interface, Universal Serial Bus **(USB)** controllers.

All detailed operating relations are shown in *Fig. 2* (PPAP-1610 System Block Diagram).



Hardware Configuration Setting

This section provides the definitions and location of jumpers, headers and connectors. All jumpers on PPAP-1610VL are configured according to the default settings set by factory, and are marked with a star ().



<u>Jumpers</u>

In general, jumpers on PPAP-1610 system board are used to select options for certain features. Some of the jumpers are configurable for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (Short) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connected".

Jumper	Default Location	Brief Description	
JP1	1-2, 3-4, 5-6, 7-8	Watchdog timer function	
JP2	JP2 1-2 RTC CMOS clear setting		
JP3	JP3 1-2, 5-6, 7-8, 9-10 Select CPU bus ratio		

(JP1) Watchdog Timer Function

JP1	Function	
1-2 Open	Disable WDT function	
1-2 Short	Enable WDT function	
3-4 Short	Allocate I/O port 543/343	
3-4 Open	Allocate I/O port 533/033	

5-6	7-8	9-10	Time-out Interval
Short	Short	Short	0.5 sec.
Short	Short	NC	1 sec.
Short	NC	Short	2 sec.
Short	NC	NC	4 sec.
NC	Short	Short	8 sec.
NC	Short	NC	16 sec.
NC	NC	Short	32 sec.
NC	NC	NC	64 sec.

(JP2) RTC CMOS Clear Jumper Setting

JP2	Function
1-2	Normal operation
2-3	Clear CMOS contents

(JP3) CPU Bus Ratio Select

BR [4]	BR [3]	BR [2]	BR [1]	BR [0]	Core/Bus Ratio
0	0	0	0	0	9.0X
0	0	0	0	1	3.0X
0	0	0	1	0	4.0X
0	0	0	1	1	10.0X
0	0	1	0	0	5.5X
0	0	1	0	1	3.5X
0	0	1	1	0	4.5X
0	0	1	1	1	9.5X
0	1	0	0	0	5.0X
0	1	0	0	1	7.0X
0	1	0	1	0	8.0X
0	1	0	1	1	6.0X
0	1	1	0	0	12.0X
0	1	1	0	1	7.5X
0	1	1	1	0	8.5X
0	1	1	1	1	6.5X
1	0	0	0	0	Reserved
1	0	0	0	1	11.0X
1	0	0	1	0	12.0X
1	0	0	1	1	Reserved

Connector

Connector	Function	
J1	Serial port D-SUB9 connector	
J2	System reset	
J5	Ethernet3 RJ-45 interface connector	
J6	Ethernet2 RJ-45 interface connector	
J7	Ethernet1 RJ-45 interface connector	
J8	Serial port 2x5 shrouded connector	
J9	Dual USB port connector	
J10	LAN LED	
J11	On-board VGA 2x5 shrouded connector	
J12	Software reset	
J13	CPLD 8-pin connector	
J14	IDE1 2x20 shrouded connector	
J15	Fan power connector: PIN1-> GND; PIN2-> +12V; PIN3-> Pull-up +3V (Reserved for sense signal)	
J16	IDE2 2x22 shrouded connector	
J17	Fan power connector: PIN1-> GND; PIN2-> +12V; PIN3-> Pull-up +3V (Reserved for sense signal)	

J18	Power input
J19	GPIO

Pin Assignments of Connectors

J1: Serial port D-SUB9 connector (COM1)

PIN No.	Signal Description
1	Data Carrier Detect (DCD)
2	Receive Data (RXD)
3	Transmit Data (TXD)
4	Data Terminal Ready (DTR)
5	Ground (GND)
6	Data Set Ready (DSR)
7	Request to Send (RTS)
8	Clear to Send (CTS)
9	Ring Indicator (RI)

J2: System reset

PIN No.	Signal Description
1	RST_SW
2	Ground

J3/J4/J5/J6/J7: Ethernet5 RJ-45 interface connector

PIN No.	Signal Description
1	ТСТ
2	TD+
3	TD-+
4	RD+
5	RD-
6	RTC
7	SPEEDLED-
8	SPEEDLED+
9	LINKLED-
10	ACTLED+

J8: Serial port 2x5 shrouded connector (COM2)

PIN No.	Signal Description		
1	Data Carrier Detect (DCD)		
2	Receive Data (RXD)		
3	Transmit Data (TXD)		
4	Data Terminal Ready (DTR)		
5	Ground (GND)		
6	Data Set Ready (DSR)		
7	Request to Send (RTS)		
8	Clear to Send (CTS)		
9	Ring Indicator (RI)		
10	N/C		

J9: Dual USB port connector

PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	N/C
3	USBD0-	4	Ground

5	USBD0+	6	USBD1+
7	Ground	8	USBD1-
9	N/C	10	+5V

J10: LAN LED (2x20 pin header)

PIN No.	Signal Description	PIN No.	Signal Description
1	LANACT1	2	LINK#_1
3	LANSPE1	4	SPEEDLED_1
5	LANACT2	6	LINK#_2
7	LANSPE2	8	SPEEDLED_2
9	LANACT3	10	LINK#_3
11	LANSPE3	12	SPEEDLED_3
13	LANACT4	14	LINK#_4
15	LANSPE4	16	SPEEDLED_4
17	LANACT5	18 LINK#_5	
19	LANSPE5	20	SPEEDLED_5

J11: On-board VGA 2x5 shrouded connector

PIN No.	Signal Description	PIN No.	Signal Description
1	RED	2	Green
3	Blue	4	VSYNC
5	HSYNC	6	MID3
7	Ground	8	MID1
9	Ground	10	N/C

J12: Factory-Default

PIN No.	Signal Description
1	SoRset
2	Ground

J13: CPLD 8-pin connector

PIN No.	Signal Description
1	+5V
2	TDO
3	TDI
4	N/C
5	N/C
6	TMS
7	Ground
8	ТСК

J14: IDE1 2x20 shroude	d connector
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PIN No.	Signal Description	PIN No.	Signal Description
1	RESET#	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	N/C
21	DMA REQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IOCHRDY	28	Pull-down
29	DMA ACK#	30	Ground
31	INT REQ	32	N/C
33	SA1	34	CBLID#
35	SA0	36	SA2
37	HDC CS0#	38	HDC CS1#
39	HDD Active#	40	Ground

J15/J17: Fan power connector

PIN No.	Signal Description
1	Ground
2	+12V
3	Pull-up 5V (Reserved for sense signal)

PIN No.	Signal Description	PIN No.	Signal Description	
1	RESET#	2	Ground	
3	Data 7	4	Data 8	
5	Data 6	6	Data 9	
7	Data 5	8	Data 10	
9	Data 4	10	Data 11	
11	Data 3	12	Data 12	
13	Data 2	14	Data 13	
15	Data 1	16	Data 14	
17	Data 0	18	Data 15	
19	Ground	20	N/C	
21	DMA REQ	22	Ground	
23	IOW#	24	Ground	
25	IOR#	26	Ground	
27	IOCHRDY	28	Pull-down	
29	DMA ACK#	30	Ground	
31	INT REQ	32	N/C	
33	SA1	34	CBLID#	
35	SA0	36	SA2	
37	HDC CS0#	38	HDC CS1#	
39	HDD Active#	40	40 Ground	
41	VCC5V	42 VCC5V		
43	Ground	44	N/C	

J17: Standard 5.25" disk power connector

J18: Power input

PIN No.	Signal Description
1	VCC5V
2	VCC5V
3	Ground
4	Ground
5	Ground
6	+12V

Use a Client Computer

Connection Using Hyper Terminal

If users use a headless PPAP-1610, which has no mouse/keyboard and VGA output connected to it, the console may be used to communicate with PPAP-1610.

Note: Terminal software may need to update for correct console output.

To access PPAP-1610 via the console, Hyper Terminal is one of the choices. Follow the steps below for the setup:

Execute HyperTerminal under C:\Program Files\Accessories\HyperTerminal

Enter a name to create new dial

Connection Description		? ×
New Connection		
Enter a name and choose an	icon for the connection:	
<u>N</u> ame:		
port		
<u>l</u> con:		
	S 🚳 🖾	X
	OK Ca	ncel

For the connection settings, make it Direct to COM1.

Connect To	? ×
ert 🚱	
Enter details for	the phone number that you want to dial:
Country code:	United States of America (1)
Ar <u>e</u> a code:	
Phone number:	
Connect using:	Direct to Com1
	Direct to Com1
	Direct to Com2 Direct to Com3
	Direct to Com4
	TCP/IP (Winsock)

Please make the port settings to Baud rate 19200, Parity None, Data bits 8, Stop bits 1

COM1 Properties	? ×
Port Settings	
	1
D 2	
Bits per second:	19200
	39400
<u>D</u> ata bits:	57600
	115200
Paritu	230400
Equity.	
<u>S</u> top bits:	1
Elow control:	Hardware 💌
Advanced	Restore Defaults
	,
	Lancel Apply

Turn on the power of PPAP-1610, after following screen was shown

🍓 port - HyperTerminal						_ 🗆 ×
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>C</u> all <u>T</u> r	ansfer <u>H</u> elp					
DF 93 D	8					
						×
Connected 0:00:15	Auto detect	Auto detect	SCROLL	CAPS	NUM	Captur /

You can then see the boot up information of PPAP-1610

🗞 p - HyperTerminal
<u>File Edit View Call Iransfer Help</u>
DF 93 DB F
Award Modular BIDS v6.00PG, An Energy Star Ally Copyright (C) 1984-2001, Award Software, Inc. Portwell, Inc. PPAP-200 BIDS Version : R1.01.42 (10172001) Main Processor : Intel Pentium III 800EB MHz(133x6.0) Memory Testing : 261120K 0K + 1024K Shared Memory Main Memory Clock is 100 MHz Primary Master : PQI IDE DiskOnModule db01.19a Primary Slave : None Secondary Master : None Secondary Slave : None
Connected 0:00:19 Auto detect 19200 8-N-1 SCROLL CAPS NUM Capture

This is the end of this section. If the terminal did not display correctly, please check the previous steps.

BIOS Setup Information

PPAP-1610 is equipped with the Award BIOS within Flash ROM. The BIOS has a built-in setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it still retains during power-off periods. When system is turned on, PPAP-1610 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. Whenever an error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the Setup program. Some errors are significant enough to abort the start-up.



Entering Setup

When message "Hit if you want to run Setup" appear during POST, after turning on or rebooting the computer, press key *immediately* to enter BIOS setup

program.

To enter Setup but fail to respond before the message disappears, please restart the system either by first turning it off and followed by turning it on (COLD START) or simply press the "RESET" button. "WARM START" (press <Ctrl>, <Alt>, and <Delete> keys simultaneously) will do as well.

When no setting is stored in BIOS or the setting is missing, a message "Press <F1> to run Setup" will appear. Then press <F1> to run Setup or resume HIFLEX BIOS Setup. User can use the keyboard to choose among options or modify the system parameters to match the options with your system. The table shown on next page will navigate through all of keystroke functions in BIOS Setup.

Key	Function
Up ()	Move to the previous item
Down ()	Move to the next item
Left ()	Move to the item on the left (menu bar)
Right ()	Move to the item on the right (menu bar)
Enter	Enter the item you desired
PgUp	Increase the numeric value or make changes
PgDn	Decrease the numeric value or make changes
	Increase the numeric value or make changes
	Decrease the numeric value or make changes
Fee	Main Menu: Quit and not save changes into CMOS
LSU	Status Page Setup Menu and Option Page Setup Menu: Exit current page and return to Main Menu
F1	General help on SETUP navigation keys
F5	Load previous values from CMOS
F6	Load the fail-safe defaults from BIOS default table
F7	Load the optimized defaults
F10	Save all the CMOS changes and exit

Keys to navigate within Setup menu

🥙 <u>Main Menu</u>

Within NAR-3060 Award BIOS CMOS Setup utility, user should start with the Main Menu. The Main Menu allows to select from eleven setup functions and two exit choices. Use arrow keys to switch among items and press <Enter> to accept or bring up the sub-menu.

Phoenix – Award BIOS CMOS Setup Utility

CMOS Setup Utility

Standard CMOS Features	Frequency /Voltage Control	
Advanced BIOS Features	Load Fail/Safe Defaults	
Advanced Chipset Features	Load Optimized Defaults	
Integrated Peripherals	Set Supervisor Password	
Power Management Setup	Set User Password	
PnP/PCI Configurations	Save & Exit Setup	
PC Health Status	Exit Without Saving	
ESC: Quit F10: Save & Exit Setup	$^{\uparrow} \downarrow \leftarrow \rightarrow$: Select Item (Shift) F2: Change Color	
Time, Date, Hard Disk Type		

NOTE: It is strongly recommended to reload the optimized default setting if CMOS is lost or BIOS is updated.

Standard CMOS Setup Menu

This setup page includes all the items within standard compatible BIOS. Use the arrow keys to highlight the item and then use the <PgUp>/<PgDn> or <+>/<-> keys to select the value or number desired in each item and press <Enter> to confirm it.

Follow command keys in CMOS Setup table to change <u>Date, Time, Drive type and Boot</u> <u>Sector Virus Protection Status</u>.

|--|

Standard CMOS Setup Utility		
Date: Wed, Jan 17 2001		
IDE Primary Master [None] IDE Primary Slave [None] IDE Secondary Master [None]		
IDE Secondary Slave [None] Video: EGA/VGA Halt On: All, but Keyboard		
Base Memory: 640K Extended Memory: 64512K Total Memory: 65536K		
ESC: Quit F1: Help PU/PD/+/-: Modify	$^{\uparrow \downarrow \leftarrow \rightarrow}$: Select Item (Shift) F2: Change Color	

Menu Selections

Item	Options	Description
Date	mm:dd:yy	Set the system date. Note that the 'Day' automatically changes when you set the date

Time	hh:mm:ss	Set the system time
Video	EGA/VGA CGA 40CGA 80MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you
Base Memory	N/A	Display the amount of conventional memory detected during boot up
Extended Memory	N/A	Display the amount of extended memory detected during boot-up
Total Memory	N/A	Display the total memory available in the system

🕗 <u>BIOS Features Setup</u>

This section allows user to configure your system for basic operation. Users will be able to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.

Screen Shot: Phoenix – Award BIOS CMOS Setup Utility

Advanced BIOS Features		
<u>Virus Warning</u> CPU Internal Cache: Enabled External Cache: Enabled CPU L2 Cache ECC Checking: Enabled Quick Power On Self Test: Enabled First Boot Device: USB-FDD	Console Redirection: Disabled Agent connect via: NULL Agent wait time (min.): 1 Agent after boot: Disabled	

🕗 Internal Cache/External Cache

These two categories speed up memory access. However, it depends on CPU/chipset design.

Enabled	Enable cache
Disabled	Disable cache

🔎 <u>Quick Power On Self Test</u>

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

Boot Up NumLock Status

Select power on state for NumLock.

The choice: Enabled/Disabled.



Gate A20 Option

This entry allows user to select how the gate A20 is handled. The gate A20 is a device used to address memory over 1 Mbytes. Originally, the gate A20 was handled via a pin on the keyboard. But now, though keyboards still provide this support, it is more common, and much faster, for the system chipset to provide support for gate A20.

Normal	Keyboard
Fast	Chipset

🕬 <u>Typematic Rate Setting</u>

Keystrokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

The choice: Enabled/Disabled.

Typematic Rate (Chars/Sec)

Set the how many number of times a second to repeat a keystroke when a key is holding down.

The choice: 6, 8, 10, 12, 15, 20, 24 and 30.

и <u>Typematic Delay (Msec)</u>

Set the delay time after the key is held down before it begins to repeat the keystroke.

The choice: 250, 500, 750 and 1000.

Security Option

Select whether the password is required every time the system boots or only when entering setup.

System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot and access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then user will be asked to enter password. Do not type anything and simply press <Enter>, it will disable security. Once the security is disabled, the system will boot up and user can enter Setup freely.

OS Select for DRAM > 64MB

Select the operating system that is running with more than 64MB of RAM on the system.

The choice: Non-OS2, OS2.

Console Redirection

Set the UNIX Console redirect to the terminal from COM1. The choice: Enabled/Disabled.

Description Baud Rate

Set the RS-232 baud rate speed.

The choice: 9600, 19200, 38400, 57600 and 115200.