









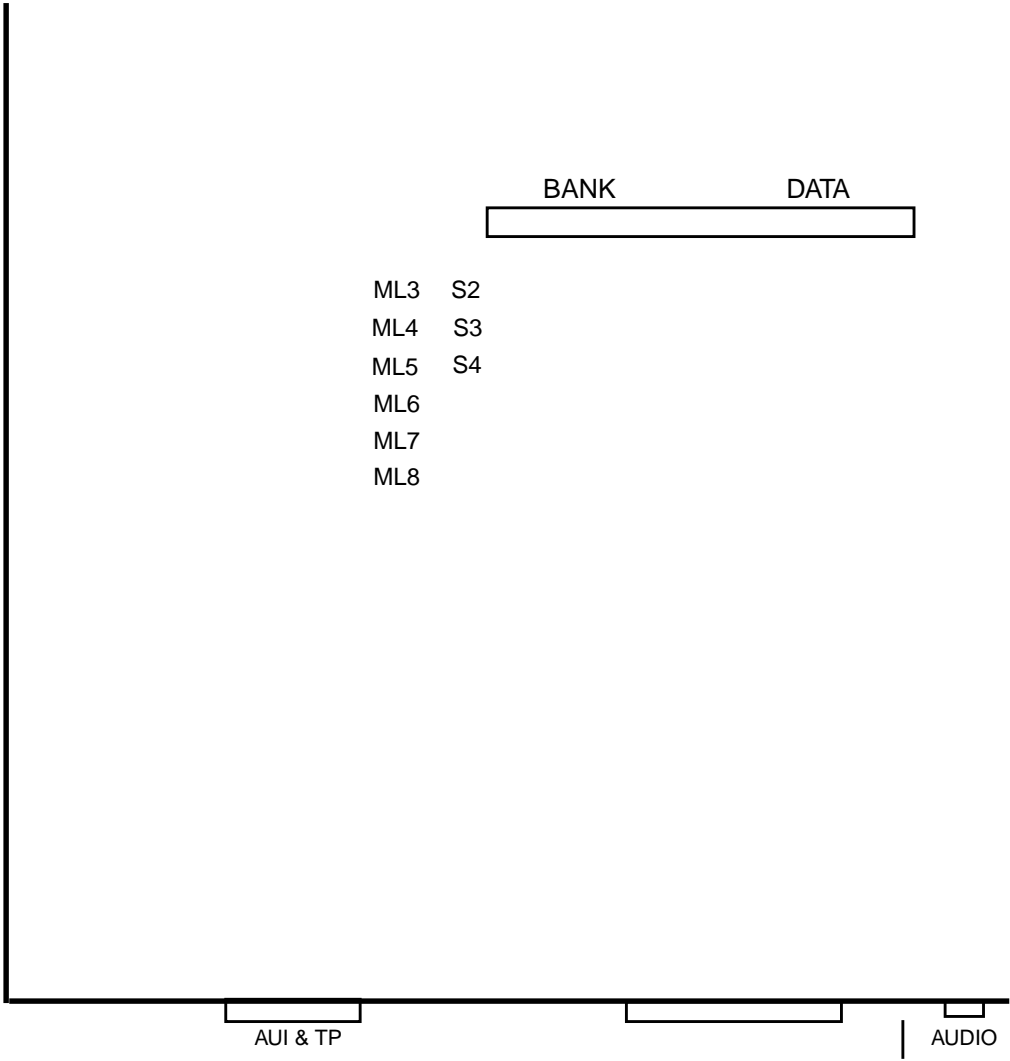


# Cycle5-IP

370-2336

0MB FRU

70MHz, 85MHz, 90MHz, 100 MHz, 110MHz

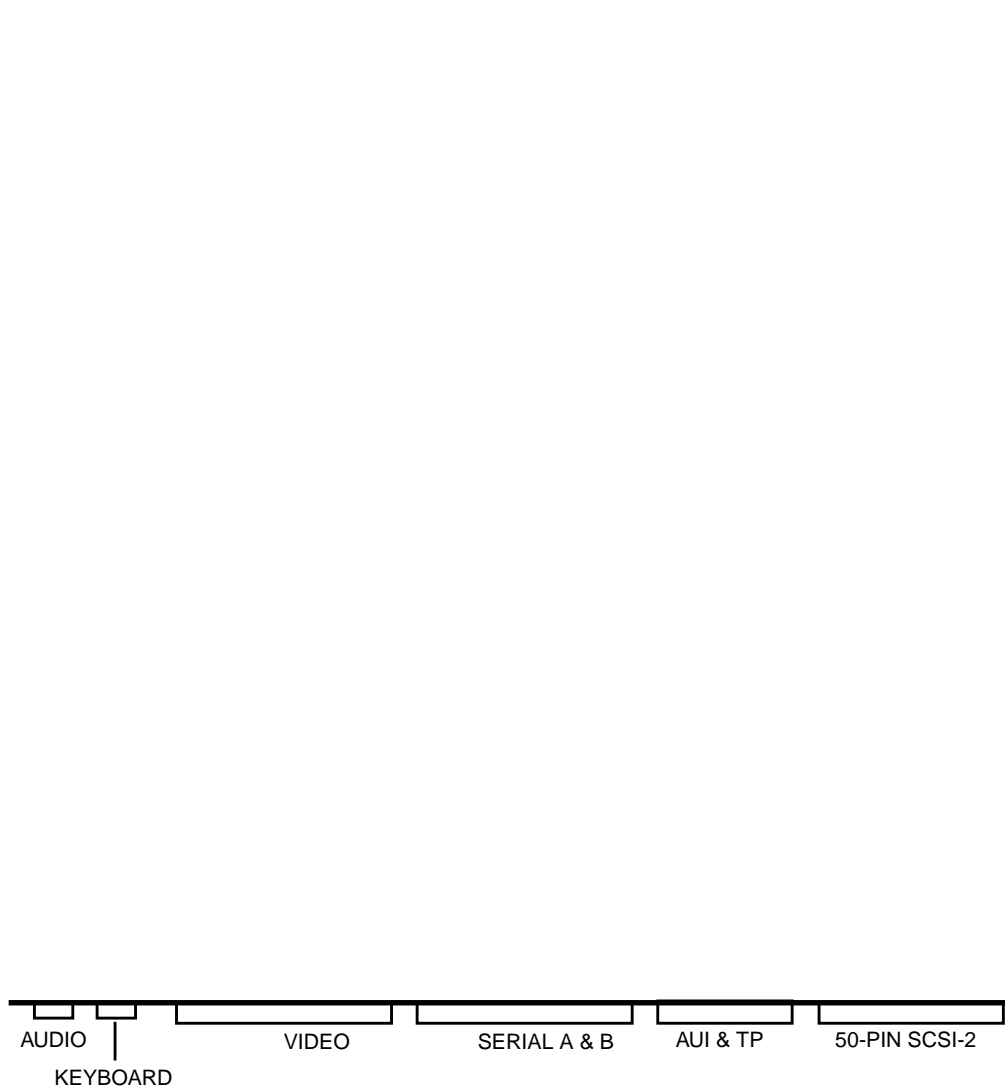


# Cycle5-IP

370-2336

0MB FRU

70MHz, 85MHz, 90MHz, 100 MHz, 110MHz



## Cycle5-IP

370-2336 370-2334

Physical Layout of memory as reported by POST

DIP SW1 #5 ON (Usually for IPX Upgrades)

(Bank 0 boots from two 72 pin SIMM's in location SO TO S1)

DIP SW1 #5 OFF (Usually for IPC Upgrades)

(Bank 0 boots from eight 30 pin SIMM's in location M1 TO M8)





# Cycle5-IP

370-2336 370-2334

